WHAT IS CLAIMED IS:

We claim:

1. A method of recovering a network timing clock of a service input of a packet-based telecommunications network, comprising the steps of:

receiving an external clock reference from a source node as an input;

providing an external clock with a frequency reference value;

dividing the external clock reference input by an integer;

configuring a status register depending on the value of the external clock frequency;

generating an integer value at the status register;

providing a divider for the generated value of the status register;

providing a digital phase locked loop to lock onto the external reference clock

2. The method of claim 1, wherein the integer that divides the external clock value is N.

3. The method of claim 1, wherein the integer value generated at the status register is Y.

4. The method of claim 1, wherein digital phase locked loop compares the external reference clock and a locally generated reference clock to produce an output reference clock.

5. The method of claim 1, wherein a numerically controlled oscillator is used to generate the local reference clock.

6. An apparatus for recovering a network timing clock of a service input of a packet-based telecommunications network, comprising the steps of:

a receiver for receiving an external clock reference from a source node as an input;

a divider for dividing the external clock reference input by an integer;

a status register to be configured depending on the value of the external clock frequency;

a generator that generates an integer value at the status register;

a divider for dividing the generated value of the status register;

a digital phase locked loop that locks onto the external reference clock

7. The apparatus of claim 6, wherein the integer that divides the external clock value is N.

8. The apparatus of claim 6, wherein the integer value generated at the status register is Y.

9. The apparatus of claim 6, wherein digital phase locked loop compares the external reference clock and a locally generated reference clock to produce an output reference clock.

10. The apparatus of claim 6, wherein a numerically controlled oscillator is used to generate the local reference clock.